WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first semiconductor layer formed above a first region of a supporting substrate with a buried oxide layer disposed therebetween, and

a second semiconductor layer formed on a second region of the supporting substrate,

wherein an interface between the supporting substrate and said second semiconductor layer is placed in substantially the same depth position as the undersurface of the buried oxide layer or in a position deeper than the buried oxide layer.

2. The semiconductor device according to claim 1, wherein the upper surface of said second semiconductor layer is positioned higher than the upper surface of the supporting substrate.

3. The semiconductor device according to claim 1, which further comprises a first element formed in said first semiconductor layer and a second element formed in said second semiconductor layer and in which an active region of said second element is formed to avoid crossing the interface between the supporting substrate and said second semiconductor layer.

4. The semiconductor device according to claim 1, wherein said second semiconductor layer is an epitaxial growth layer and the interface between the supporting substrate and said second semiconductor layer is an

interface between the supporting substrate and said epitaxial growth layer.

5. The semiconductor device according to claim 1, wherein the interface between the supporting substrate and said second semiconductor layer is an interface of bonding the supporting substrate and said second semiconductor layer.

6. The semiconductor device according to claim 1, wherein the supporting substrate and said first and second semiconductor layers are formed of silicon and the buried oxide layer is formed of silicon oxide.

7. The semiconductor device according to claim 1, wherein the concentration of oxygen in a portion of the supporting substrate which lies near the interface between the supporting substrate and said second semiconductor layer is lower than the concentration of oxygen in a portion of the supporting substrate which lies near and directly under the buried oxide layer.

8. The semiconductor device according to claim 3, wherein said second element includes a trench type memory cell of a DRAM and the interface between the supporting substrate and said second semiconductor layer is set at substantially the same height as the lower surface of the buried oxide layer and crosses a collar oxide film of a trench capacitor of the trench type memory cell.

9. The semiconductor device according to claim 3,

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wherein said second element includes a trench type memory cell of a DRAM and the interface between the supporting substrate and said second semiconductor layer is set at substantially the same height as the lower surface of the buried oxide layer and crosses a trench capacitor of the trench type memory cell.

10. The semiconductor device according to claim 3, wherein said second element includes a trench type memory cell of a DRAM and the interface between the supporting substrate and said second semiconductor layer is set at substantially the same height as the lower surface of the buried oxide layer and crosses a portion which lies deeper than a trench capacitor of the trench type memory cell.

11. The semiconductor device according to claim 3, wherein said second element includes a trench type memory cell of a DRAM and the interface between the supporting substrate and said second semiconductor layer is set in a portion which lies deeper than the buried oxide layer and crosses a trench capacitor of the trench type memory cell.

12. The semiconductor device according to claim 3, wherein said second element includes a trench type memory cell of a DRAM and the interface between the supporting substrate and said second semiconductor layer is set in a portion which lies deeper than the buried oxide layer and crosses a portion which lies

deeper than a trench capacitor of the trench type memory cell.

13. A semiconductor device manufacturing method comprising:

selectively removing portions of a buried oxide layer and first semiconductor layer in an SOI substrate having the first semiconductor layer formed above a semiconductor substrate with the buried oxide layer disposed therebetween and exposing part of the semiconductor substrate,

removing an exposed region of the semiconductor substrate in a depth direction, and

burying a second semiconductor region in the region from which part of the semiconductor substrate has been removed in the depth direction.

14. The semiconductor device manufacturing method according to claim 13, further comprising respectively forming first and second elements in the first and second semiconductor layers.

15. The semiconductor device manufacturing method according to claim 13, wherein removing the exposed region of the semiconductor substrate in the depth direction is performed by use of a wet etching method using a solution.

16. The semiconductor device manufacturing method according to claim 13, wherein burying the second semiconductor region in the region from which part of

the semiconductor substrate has been removed in the depth direction is performed by use of an epitaxial growth method.

17. The semiconductor device manufacturing method according to claim 13, further comprising forming a sidewall protection film on a sidewall of the region from which part of the semiconductor substrate has been removed in the depth direction after removing the exposed region of the semiconductor substrate in the depth direction.

18. The semiconductor device manufacturing method according to claim 17, wherein the sidewall protection film is formed of silicon nitride.

19. The semiconductor device manufacturing method according to claim 13, further comprising subjecting the exposed surface of the semiconductor substrate to a hydrogen-annealing process after removing the exposed region of the semiconductor substrate in the depth direction.

20. A semiconductor device manufacturing method comprising:

selectively removing portions of a buried oxide layer and first semiconductor layer in an SOI substrate having the first semiconductor layer formed above a semiconductor substrate with the buried oxide layer disposed therebetween,

forming a sidewall protection film on a sidewall

of the first semiconductor layer,

removing a portion of the remaining buried oxide layer and exposing the surface of the semiconductor substrate, and

forming a second semiconductor layer on the exposed surface of the semiconductor substrate.

21. The semiconductor device manufacturing method according to claim 20, further comprising respectively forming first and second elements in the first and second semiconductor layers.

22. The semiconductor device manufacturing method according to claim 20, wherein exposing the surface of the semiconductor substrate is performed by use of a wet etching method using a solution.

23. The semiconductor device manufacturing method according to claim 20, wherein forming the second semiconductor layer is performed by use of an epitaxial growth method.

24. The semiconductor device manufacturing method according to claim 20, wherein the sidewall protection film is formed of silicon nitride.

25. The semiconductor device manufacturing method according to claim 20, further comprising subjecting the exposed surface of the semiconductor substrate to a hydrogen-annealing process after exposing the surface of the semiconductor substrate.